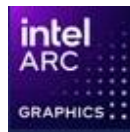


# SPARKLE®

## SBP60W-24G

Professional PCIe Graphics

4 x DisplayPort



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## **1. Specification**

<b>Model Name</b>	<b>SBP60W-24G</b>
<b>Graphics Engine</b>	Intel® Arc™ Pro B60
<b>Process Node</b>	5 nm
<b>GPU Clock</b>	2400MHz
<b>Graphics Memory</b>	192-bit, 24 GB, GDDR6
<b>Memory Clock</b>	19 Gbps
<b>Bus Interface</b>	PCI Express® 5.0 (x8)
<b>Xe-core</b>	20
<b>Intel® XMMAI engines</b>	160
<b>Shader Processing Units</b>	2560
<b>Floating Point Performance (FP32)</b>	12.28 TFLOPs
<b>GPU Peak TOPS (int8)</b>	197 TOPS
<b>DirectX® Capability</b>	DirectX® 12
<b>OpenGL™</b>	OpenGL™ 4.6
<b>OpenCL™</b>	OpenCL™ 3.0
<b>VULKAN™</b>	VULKAN™ 1.3
<b>Unified Video Decoder</b>	Xe Media Engine
<b>BIOS Mode</b>	UEFI
<b>Display Interface</b>	4 x DisplayPort 2.1
<b>Maximum Resolution</b>	DisplayPort: 7680x4320
<b>Power Consumption</b>	200 W
<b>Operating Temperature</b>	0°C ~ 45°C
<b>Dimension</b>	289 x 112 x 42 mm

\* The product specifications are subject to change without notice.

## 2. Functional Overview

### 2.1. Graphics Memory

B60 memory subsystem supports GDDR6 technology with the data rate 19Gbps. The total capacity of graphics memory is up to 24GB in x8 config (Clamshell). B60 memory controller trains the memory interface to achieve the best performance.

### 2.2. Media Support

B60 implements multiple media video codecs in hardware as well as a rich set of image processing algorithms. Multi-format hardware assisted decode/encode pipeline and Mid-Level Cache (MLC) are used for superior high definition playback, video quality, and improved 3D performance and media.

#### Hardware Accelerated Video Decode

B60 implements a high-performance and low-power hardware acceleration for video decoding operations for multiple video codecs.

The hardware decode is exposed by the graphics driver using the following APIs:

- Direct3D\* 9 Video API (DXVA2)
- Direct3D\* 12 Video API
- Intel® Media SDK
- MFT (Media Foundation Transform) filters
- Intel® VA API

B60 supports full HW accelerated video decoding for VC/VC1/MPEG2/HEVC/VP9/JPEG/AV1.

#### NOTE

Actual performance depends on content bit rate, and memory frequency. Hardware decode for H264 SVC is not supported.

#### Hardware Accelerated Video Encode

B60 implements a low-power low-latency fixed function encoder and a high-quality customizable encoder with hardware assisted motion estimation engine which supports AVC, MPEG-2, HEVC, and VP9.

The hardware encode is exposed by the graphics driver using the following APIs:

- Intel® Media SDK
- MFT (Media Foundation Transform) filters

Supports full hardware accelerated video encoding for AVC/MPEG2/HEVC/VP9/JPEG.

### Hardware Accelerated Video Processing

There is hardware support for image processing functions such as:

- De-interlacing
- Film cadence detection
- Advanced Video Scaler (AVS)
- Detail enhancement
- Image stabilization
- Gamut compression
- HD adaptive contrast enhancement
- Skin tone enhancement
- Total color control
- Chroma de-noise
- SFC (Scalar and Format Conversion)
- Memory compression
- Localized Adaptive Contrast Enhancement (LACE)
- Spatial de-noise
- Out-Of-Loop De-blocking (from AVC decoder)
- 16 bpc support for de-noise/de-mosaic

The hardware video processing is exposed by the graphics driver using the following APIs:

- Direct3D\* 9 Video API (DXVA2)
- Direct3D\* 12 Video API
- Intel® Media SDK
- MFT (Media Foundation Transform) filters
- Intel® IGCC SDK

#### NOTE

Not all features are supported by all the above APIs.

### 2.3. Display System

#### Display Technologies Support

Technology	Standard
DisplayPort* 2.1,1.4	VESA* DisplayPort* Standard 2.1,1.4 VESA* DisplayPort* PHY Compliance Test Specification 2.1,1.4 VESA* DisplayPort* Link Layer Compliance Test Specification 2.1,1.4
HDMI2.1 FRL, HDMI2.1 TMDS Compatible	High-Definition Multimedia Interface Specification Version 2.1 High-Definition Multimedia Interface Specification Version 2.1 TMDS Compatible

#### Display Configuration

##### Display Ports Availability and Link Rate

Port	Link Rate
DDI 1	DP* up to UHBR13.5 (13.5 Gbps)
DDI 2	DP* up to UHBR10 (10 Gbps) HDMI* up to 12 Gbps
DDI 3	DP* up to UHBR10 (10 Gbps) HDMI* up to 12 Gbps
DDI 4	DP* up to UHBR10 (10 Gbps)

#### Display Features

##### General Capabilities

- Up to four simultaneous displays
- Audio stream support on external ports
- Color space conversion
- HDR support

##### Multiple Display Configurations

The following multiple display configuration modes are supported (with appropriate driver software):

- Single Display is a mode with one display port activated to display the output to one display device.
- Display Clone is a mode with up to four display ports activated to drive the display content of same color depth setting but potentially different refresh rate and resolution settings to all the active display devices connected.

- Extended Desktop is a mode with up to four display ports activated to drive the content with potentially different color depth, refresh rate, and resolution settings on each of the active display devices connected.

### Simultaneous Display Support

Simultaneous Displays	Maximum Resolution <sup>3</sup>
1 <sup>1</sup>	7680x4320@120Hz HDR (Compressed) <sup>2</sup>
2 <sup>1</sup>	7680x4320@60Hz HDR
3 or 4 <sup>1</sup>	3840x2160@120Hz HDR

Notes:

1. Resolution support is subject to memory bandwidth availability.
2. Resolution applicable for HDMI 2.1 FRL displays only.
3. These are using VESA Coordinated Video Timings (CVT) with reduced blanking.
4. 7680x4320@120Hz and 7680x4320@60Hz are DSC capable displays.

### High-bandwidth Digital Content Protection (HDCP)

HDCP is the technology for protecting high-definition content against unauthorized copy or unreceptive between a source (computer, digital set top boxes, and so on) and the sink (panels, monitor, and TVs). BMG SoC supports both HDCP 2.3 and 1.4 content protection over wired displays (HDMI\* and DisplayPort\*). The HDCP 1.4/2.3 keys are integrated into BMG SoC and customers are not required to physically configure or handle the keys.

## 2.4. DisplayPort (DP) Features

- Support main link of 1, 2, or 4 data lanes
- Aux channel for Link/Device management
- Support up to 36 BPP (Bit per Pixel)
- Support SSC
- Support YCbCR 4:4:4, YCbCR 4:2:0, and RGB color format
- Support MST (Multi-Stream Transport)
- Support VESA DSC 1.2a
  1. RGB, YUV 4:4:4, YUV 4:2:2 and YUV 4:2:0
- Adaptive Sync

### DisplayPort\* Maximum Resolution

Standard	Link Rate	Maximum Resolution
DP1.4	HBR3	7680x4320@60Hz HDR (Compressed)
DP2.1	UHBR10	7680x4320@60Hz HDR or 5120x2160@240Hz HDR
DP2.1	UHBR13.5	3840x2160@360Hz HDR or 5120x2160@240Hz HDR or 7680x4320@60Hz HDR

#### Notes:

1. Maximum resolution is based on the implementation of 4 lanes at respective data rate.
2. Resolution support is subject to memory bandwidth availability.
3. SSC is supported only on DP and not on HDMI.
4. These are using VESA Coordinated Video Timings (CVT) with reduced blanking

## 2.5. HDMI Features

- DDC (Display Data Channel) channel
- Support YCbCR 4:4:4, YCbCR 4:2:0, and RGB color format
- Support up to 36 bpp (bit per pixel)
- Adaptive Sync supported on HDMI 2.1

### HDMI\* Maximum Resolution

Standard	Maximum Resolution
HDMI 2.1 <sup>1</sup>	7680x4320@120Hz HDR (Compressed)
HDMI 2.1 TMDS Compatible	3840x2160@60Hz HDR
HDMI 1.4	3840x2160@30Hz

#### Notes:

1. Maximum resolution is supported in HDMI FRL mode with 12Gbps per lane
2. Resolution support is subject to memory bandwidth availability.
3. Refer the HDMI.org for the latest HDMI2.1 Specification

### Integrated Audio

HDMI\* and DisplayPort\* interfaces carry audio along with the video. BMG SoC supports four High Definition audio streams on four digital ports simultaneously.

## 2.6. PCI Express Support Features

B60 PCI Express\* interface is a 8-lane (x8) port. B60 supports the following:

- 100-MHz differential clock as PCI Express\* reference clock
- Power Management Event (PME) functions

**PCI Express\* Maximum Transfer Rate and Theoretical Bandwidth**

PCI Express* Generation	Encoding	Maximum Transfer Rate [GT/s]	Theoretical Bandwidth [GB/s]
			x8
Gen 1	8b/10b	2.5	2.0
Gen 2	8b/10b	5	4.0
Gen 3	128b/130b	8	7.88
Gen 4	128b/130b	16	15.75
Gen 5	128b/130b	32	31.5

## 3. PIN Assignment and Description

Pin #	Side B Connector		Side A Connector	
	Name	Description	Name	Description
1	+12v	+12 volt power	PRSNT#1	Hot plug presence detect
2	+12v	+12 volt power	+12v	+12 volt power
3	RSVD	Reserved	+12v	+12 volt power
4	GND	Ground	GND	Ground
5	SMCLK	SMBus clock	JTAG2	TCK
6	SMDAT	SMBus data	JTAG3	TDI
7	GND	Ground	JTAG4	TDO
8	+3.3v	+3.3 volt power	JTAG5	TMS
9	JTAG1	+TRST#	+3.3v	+3.3 volt power
10	3.3Vaux	3.3v volt power	+3.3v	+3.3 volt power
11	WAKE#	Link Reactivation	PWRGD	Power Good

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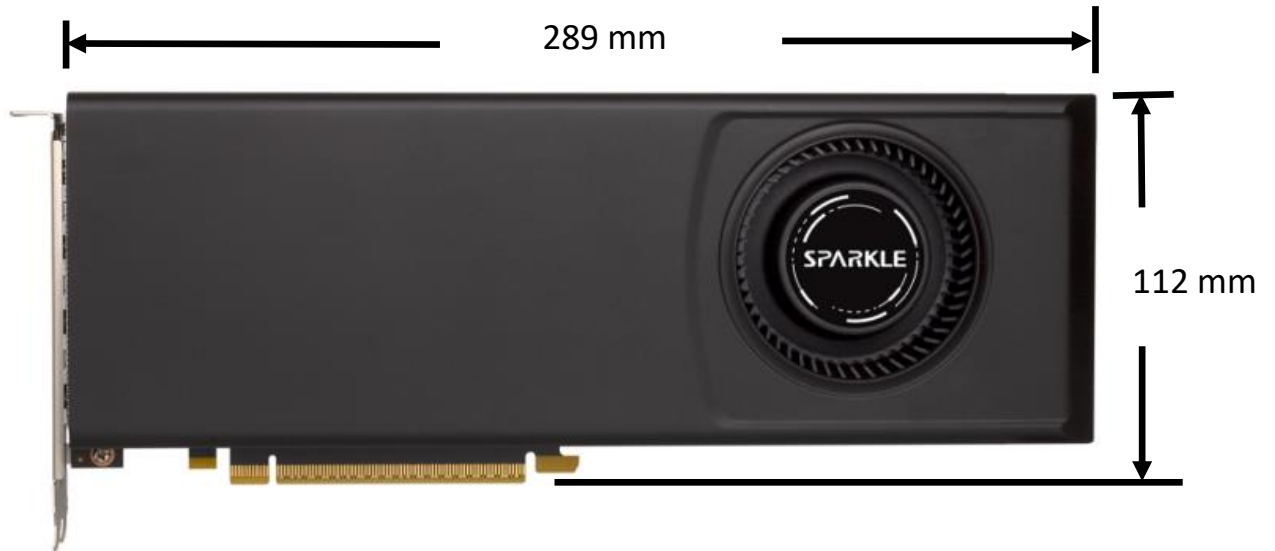
Pin #	Side B Connector		Side A Connector	
	Name	Description	Name	Description
<b>Mechanical Key</b>				
12	RSVD	Reserved	GND	Ground
13	GND	Ground	REFCLK+	Reference Clock Differential pair
14	HSOp(0)	Transmitter Lane 0,	REFCLK-	
15	HSOn(0)	Differential pair	GND	Ground
16	GND	Ground	HSIp(0)	Receiver Lane 0, Differential pair
17	PRSNT#2	Hotplug detect	HSIn(0)	
18	GND	Ground	GND	Ground
19	HSOp(1)	Transmitter Lane 1,	RSVD	Reserved
20	HSOn(1)	Differential pair	GND	Ground
21	GND	Ground	HSIp(1)	Receiver Lane 1, Differential pair
22	GND	Ground	HSIn(1)	
23	HSOp(2)	Transmitter Lane 2,	GND	Ground
24	HSOn(2)	Differential pair	GND	Ground
25	GND	Ground	HSIp(2)	Receiver Lane 2, Differential pair
26	GND	Ground	HSIn(2)	
27	HSOp(3)	Transmitter Lane 3,	GND	Ground
28	HSOn(3)	Differential pair	GND	Ground
29	GND	Ground	HSIp(3)	Receiver Lane 3, Differential pair
30	RSVD	Reserved	HSIn(3)	
31	PRSNT#2	Hot plug detect	GND	Ground
32	GND	Ground	RSVD	Reserved
33	HSOp(4)	Transmitter Lane 4,	RSVD	Reserved
34	HSOn(4)	Differential pair	GND	Ground
35	GND	Ground	HSIp(4)	Receiver Lane 4, Differential pair
36	GND	Ground	HSIn(4)	
37	HSOp(5)	Transmitter Lane 5,	GND	Ground

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Pin	Side B Connector		Side A Connector	
	Name	Description	Name	Description
38	HSON(5)	Differential pair	GND	Ground
39	GND	Ground	HSIp(5)	Receiver Lane 5, Differential pair
40	GND	Ground	HSIn(5)	
41	HSoP(6)	Transmitter Lane 6, Differential pair	GND	Ground
42	HSON(6)		GND	Ground
43	GND	Ground	HSIp(6)	Receiver Lane 6, Differential pair
44	GND	Ground	HSIn(6)	
45	HSoP(7)	Transmitter Lane 7, Differential pair	GND	Ground
46	HSON(7)		GND	Ground
47	GND	Ground	HSIp(7)	Receiver Lane 7, Differential pair
48	PRSNT#2	Hot plug detect	HSIn(7)	
49	GND	Ground	GND	Ground

## 4. Board Configuration

### 4.1 Board Dimension

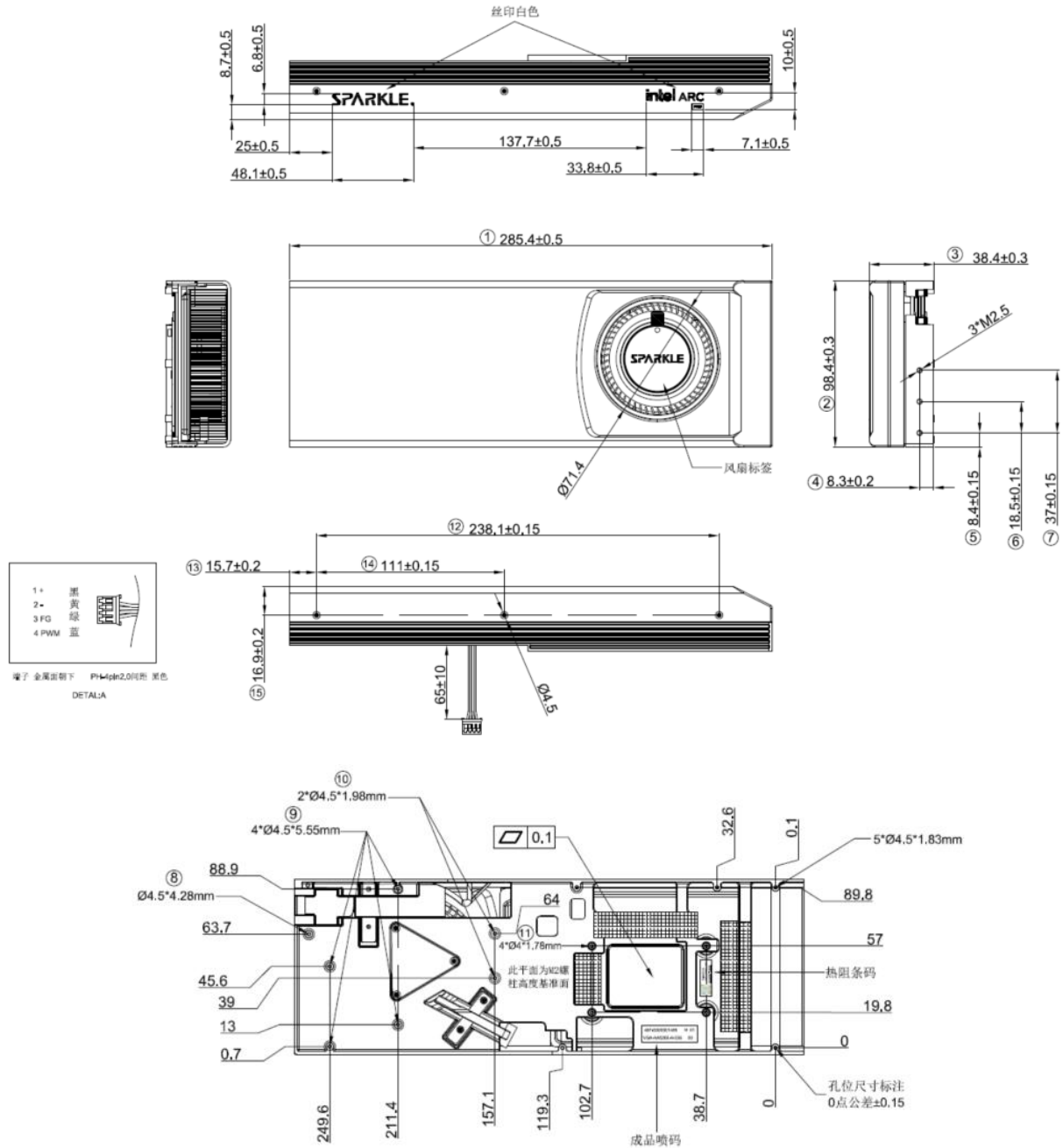


### 4.2 Display Interface



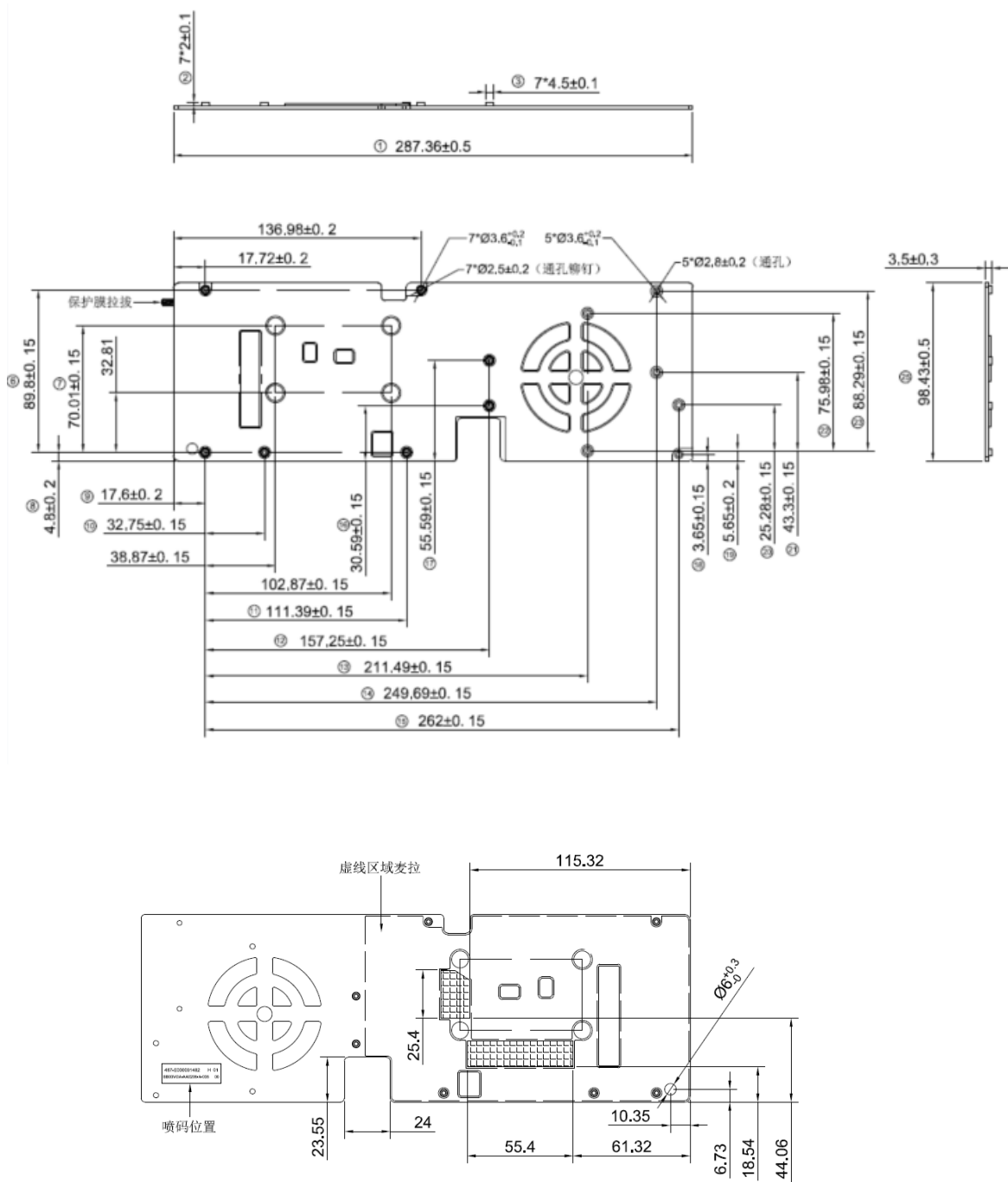
## 5. Thermal Mechanism

### 5.1 Fan Thermal Module (Cooler)



(Unit : mm)

## 5.2 Fan Thermal Module (Backplane)



(Unit : mm)

## Change log list

<b>Rev.</b>	<b>Data</b>	<b>History</b>
1.0	2025/08/04	SBP60W-24G datasheet